CLAIMS:

1. A clock selection device adapted to select one of a pair of clock sources onto an output clock line, comprising:

a first input clock line coupled to a first clock source;

a second input clock line coupled to a second clock source, the second clock source asynchronous to the first clock source; and

a clock selection logic adapted to select from the first input clock line and the second input clock line, producing an internal clock line coupled to the output clock line.

2. The clock selection device of claim 1, the first clock source having a first frequency and the second clock source having a second frequency, the second frequency independent of the first frequency.

3. The clock selection device of claim 1, further comprising:

a clock synchronization logic coupled to the first input clock line, the second input clock line, and the clock selection logic, adapted to synchronize the first input clock line, the second input clock line, and the clock selection logic, such that the internal clock line is glitch free.

4. The clock selection device of claim 3, the clock synchronization logic comprising:

a first clock synchronization block, coupled to the first clock source, adapted to synchronize the first clock source and the clock selection logic; and

a second clock synchronization block, coupled to the second clock source, adapted to synchronize the second clock source and the clock selection logic.

5. The clock selection device of claim 4, the clock synchronization logic further comprising:

a first clock reset signal, synchronized to the first clock signal, adapted to reset the first clock synchronization block; and

a second clock reset signal, synchronized to the second clock signal, adapted to reset the second clock synchronization block,

wherein the first clock reset signal and the second clock reset signal can be asserted to prevent meta-stability of the clock synchronization logic.

6. The clock selection device of claim 3, wherein the clock synchronization logic is scalable to produce a predetermined delay time between the assertion of the clock select signal and the selection onto the output line by the clock selection logic.

7. The clock selection device of claim 1, wherein the clock selection logic comprises a multiplexer with two clock input lines.

8. The clock selection device of claim 7, wherein the multiplexer switches only when both clock input lines of the multiplexer are at the same assertion level.

9. The clock selection device of claim 1, further comprising:

a clock selection signal, asynchronous to the first clock source and the second clock source, adapted to cause the clock selection logic to select one of the first input clock source and the second input clock source onto the internal clock line, selecting the first input clock source when the clock selection signal is asserted and the second input clock source when the clock selection signal is deasserted.

10. The clock selection device of claim 3, the clock synchronization logic comprising:

an OR gate coupled to a clock select line and an internal feedback line of the clock synchronization logic;

a first plurality of flip-flops coupled to the output of the OR gate and the second input clock line, producing a clock switch line adapted to cause the clock selection logic to switch between the first clock source and the second clock source;

an AND gate coupled to the clock select line and the clock switch line; and

a second plurality of flip-flops coupled to the output of the AND gate and the first input clock line, the output of the second plurality of flip-flops coupled to the internal feedback line.

11. The clock selection device of claim 10, the clock selection logic comprising:

an AND gate coupled to the internal feedback line and the first input clock line.

12. The clock selection device of claim 10, the clock synchronization logic further comprising:

an inverter coupled to the first input clock line producing an inverted first input clock line coupled to the first plurality of flip-flops; and

an inverter coupled to the second input clock line producing an inverted second input clock line coupled to the second plurality of flip-flops; and

the clock selection logic comprising:

a NAND gate coupled to the internal feedback line and the inverted first input clock line.

13. The clock selection device of claim 1, further comprising:

a buffer coupled to the internal clock line, producing a buffered output clock signal.

14. A processor-based device comprising:

a processor;

a plurality of communication controllers coupled to the processor, each of the plurality of communication controllers comprising:

a first clock source;

a second clock source asynchronous to the first clock source; and

a clock selection device coupled to the first clock source and the second clock source comprising:

a first input clock line coupled to the first clock source;

a second input clock line coupled to the second clock source; and

a clock selection logic adapted to select from the first input clock line and the second input clock line, producing an internal clock line.

15. The clock selection device of claim 14, the first clock source having a first frequency and the second clock source having a second frequency, the second frequency independent of the first frequency.

16. The processor-based device of claim 14, the clock selection device further comprising:

a clock synchronization logic coupled to the first input clock line, the second input clock line, and the clock selection logic, adapted to synchronize the first input clock line, the second input clock line, and the clock selection logic, such that the internal clock line is glitch free.

17. The processor-based device of claim 16, the clock synchronization logic comprising:

a first clock synchronization block, coupled to the first clock source, adapted to synchronize the first clock source and the clock selection logic;

a second clock synchronization block, coupled to the second clock source, adapted to synchronize the second clock source and the clock selection logic.

18. The processor-based device of claim 17, the clock synchronization logic further comprising:

a first clock reset signal, synchronized to the first clock signal, adapted to reset the first clock synchronization block; and

a second clock reset signal, synchronized to the second clock signal, adapted to reset the second clock synchronization block,

wherein the first clock reset signal and the second clock reset signal can be asserted to prevent meta-stability of the clock synchronization logic.

19. The processor-based device of claim 16, wherein the clock synchronization logic is scalable to produce a predetermined delay time between the assertion of the clock select signal and the selection onto the output line by the clock selection logic.

20. The processor-based device of claim 14, wherein the clock selection logic comprises a multiplexer with two input lines.

21. The processor-based device of claim 20, wherein the multiplexer switches only when both input lines of the multiplexer are at the same assertion level.

22. The processor-based device of claim 14, the clock selection device further comprising:

a clock selection signal, asynchronous to the first clock source and the second clock source, adapted to cause the clock selection logic to select one of the first input clock source and the second input clock source onto the internal clock line, selecting the first input clock source when the clock selection signal is asserted and the second input clock source when the clock selection signal is unasserted.

23. The processor-based device of claim 22, the clock selection device further comprising:

a clock synchronization logic coupled to the first input clock line, the second input clock line, and the clock selection logic, adapted to synchronize the first input clock line, the second input clock line, and the clock selection logic, such that the internal clock line is glitch free.

24. The processor-based device of claim 23, the clock synchronization logic comprising:

an OR gate coupled to a clock select line and an internal feedback line of the clock synchronization logic;

a first plurality of flip-flops coupled to the output of the OR gate and the second input clock line, producing a clock switch line adapted to cause the clock selection logic to switch between the first clock source and the second clock source;

an AND gate coupled to the clock select line and the clock switch line; and

a second plurality of flip-flops coupled to the output of the AND gate and the first input clock line, the output of the second plurality of flip-flops coupled to the internal feedback line.

25. The processor-based device of claim 24, the clock selection logic comprising:

an AND gate coupled to the internal feedback line and the first input clock line.

26. The processor-based device of claim 24, the clock synchronization logic further comprising:

an inverter coupled to the first input clock line producing an inverted first input clock line coupled to the first plurality of flip-flops; and

an inverter coupled to the second input clock line producing an inverted second input clock line coupled to the second plurality of flip-flops; and

the clock selection logic comprising:

a NAND gate coupled to the internal feedback line and the inverted first input clock line.

27. The processor-based device of claim 14, the clock selection device further comprising:

a buffer coupled to the internal clock line, producing a buffered output clock signal on the output clock line.

28. A method of selecting one of a pair of clock sources onto a single output clock line, comprising the steps of:

(a) receiving a first input clock signal from a first clock source;

(b) receiving a second input clock signal from a second clock source, the second input clock signal asynchronous to the first input clock signal; and

(c) connecting one of first clock signal or the second clock signal to an internal clock line coupled to the output clock line.

29. The method of claim 28, the first clock source having a first frequency and the second clock source having a second frequency, the second frequency independent of the first frequency.

30. The method of claim 28, furthering comprising the step of:

buffering the internal clock line to generate the output clock line.

31. The method of claim 28, further comprising the steps of:

synchronizing the first input clock signal, the second input clock signal, and step (c), such that the output clock line is glitch free.

32. The method of claim 31, the step of synchronizing comprising the step of:

delaying step (c) for a predetermined amount of time.

33. The method of claim 31, the step of synchronizing comprising the steps of:

resetting a synchronization logic with a first reset signal synchronous to the first clock signal; and

resetting the synchronization logic with a second reset signal synchronous to the second clock signal.

34. The method of claim 28, step (c) comprising the steps of:

(c1) receiving a clock select signal asynchronous to the first clock signal and the second clock signal; and

(c2) connecting the first clock signal to the output clock line when the clock select signal is asserted;

(c3) connecting the second clock signal to the output clock line when the clock select signal is deasserted;

(c4) synchronizing the first input clock signal, the second input clock signal, and steps (c2) and (c3), such that the output clock line is glitch free.

35. A clock switching mechanism with guaranteed stability, comprising:

a clock switching means for switching a clock source of a first clock source and a second clock source to an output clock line, the second clock source asynchronous to the first clock source; and

a clock synchronization means coupled to the first and the second clock sources and the clock switching means, the clock synchronization means guaranteeing the output clock line is glitch free.

36. The clock switching mechanism of claim 35, the clock synchronization means comprising:

a first reset means synchronized to the first clock source for resetting the clock synchronization means; and

a second reset means synchronized to the second clock source for resetting the clock synchronization means,

wherein the first reset means and the second reset means can prevent meta-stability of the clock synchronization means.

37. The clock switching mechanism of claim 35, the first clock source having a first frequency and the second clock source having a second frequency, the second frequency independent of the first frequency.

38. The clock switching mechanism of claim 35, the clock synchronization means comprising:

a first synchronization means coupled to the first clock source for synchronizing the first clock source to the clock switching means;

a second synchronization means coupled to the second clock source for synchronizing the second clock source to the clock switching means;

a clock selection means coupled to the first synchronization means and the second synchronization means for causing the clock switching means to switch between the first clock source and the second clock source;

a first feedback means coupled to the clock selection means and the first synchronization means for synchronizing the second synchronization means and the clock selection means; and

a second feedback means coupled to the clock selection means and the second synchronization means for synchronizing the first synchronization means and the clock selection means.